

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: )  
JUSTIN K. BRASK )  
MARK L. DOCZY )  
JACK KAVALIEROS )  
MATTHEW V. METZ )  
CHRIS E. BARNS )  
UDAY SHAH )  
SUMAN DATTA )  
CHRISTOPHER D. THOMAS )  
ROBERT S. CHAU )  
Serial No.: unknown ) Art Unit: unknown  
Filed: unknown ) Examiner: unknown  
For: A CMOS DEVICE WITH ) Attorney Docket: P18244  
METAL AND SILICIDE GATE )  
ELECTRODES AND A )  
METHOD FOR MAKING IT )

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is being submitted under 37 C.F.R. §1.97(b). Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the references cited on that form. It is respectfully requested that the cited references be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement constitutes prior art or is otherwise material to patentability.

Respectfully submitted,

Dated: December 22, 2003

  
Mark V. Seeley  
Reg. No. 32,299

Intel Corporation  
Mail Stop SC4-202  
2200 Mission College Blvd.  
Santa Clara, CA 95052-8119  
(408) 765-7382

"Express Mail" mailing label number: EU 409342011 US  
Date of Deposit: December 29, 2003  
I hereby state that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Commissioner for Patents,  
PO Box 1450, Alexandria, Virginia 22313-1450  
Teresa Edwards  
(Typed or printed name of person mailing paper or fee)  
Teresa Edwards  
(Signature of person mailing paper or fee)  
December 29, 2003  
(Date signed)

Form PTO-1449 (Modified)		Atty Docket No.: 42P18244		Serial No.: Unknown			
List of Patents and Publications Statement (Use several sheets if necessary)				Applicant: Justin K. Brask et al.			
				Filing Dat : Herewith			
REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS				
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate	
	AA	6,063,698	Tseng et al.	438	585		
	AB	6,184,072	Kaushik et al.	438	197		
	AC	6,420,279	Ono et al.	438	785		
	AD	6,475,874	Xiang et al.	438	396		
	AE	6,514,828	Ahn et al.	438	240		
	AF	6,544,906	Rotondaro et al.	438	785		
	AG	6,617,209	Chau et al.	438	240		
	AH	6,617,210	Chau et al.	438	240		
	AI	US2002/0197790	Kizilyalli et al.	438	240		
	AJ	US2003/032303	Yu et al.	438	770		
	AK	US2003/0045080	Visokay et al.	438	591		
FOREIGN PATENT DOCUMENTS							
		Document No.	Date	Country	Class	Sub-Class	Translation
	AL						
	AM						
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)							
	AN	Polishchuk et al. "Dual Workfunction CMOS Gate Technology Based on Metal Interdiffusion," www.eesc.berkeley.edu, 1 page					
	AO	Doug Barlage et al., "High-Frequency Response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics", 2001 IEEE, 4 pages.					
	AP	Lu et al., "Dual-Metal Gate Technology for Deep-Submicron CMOS Devices", dated April 29, 2003, 1 page.					
	AQ	Schwantes et al., "Performance Improvement of Metal Gate CMOS Technologies with Gigabit Feature Sizes", Technical University of Hanburg-Harburg, 5 pages.					
	AR	Doczy et al., "Integrating N-type and P-type Metal Gate Transistors", Serial No. 10/327,293, Filed December 20, 2002					
	AS	Brask et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/387,303, Filed March 11, 2003					
	AT	Brask et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/391,816, Filed March 18, 2003					
	AU	Chau et al., "A Method for Making a Semiconductor Device Having a Metal Gate Electrode", Serial No. 10/431,166, Filed May 6, 2003					
	AV	Brask et al. "A Selective Etch Process for Making a Semiconductor Device Having a High-K Gate Dielectric," Serial No. 10/652,546, filed August 28, 2003					
	AW	Brask et al. "A Method for Making a Semiconductor Device Having a High-K Gate Dielectric," Serial No. 10/642,796, filed August 28, 2003					
	AX	Brask, "Methods and Compositions for Selectively Etching Metal Films and Structures," Serial No. 10/658,225, filed September 8, 2003					
	AY	Brask et al., "A Method for Making a Semiconductor Device that Includes a Metal Gate Electrode", Serial No. Unknown, Filed December 18, 2003					
	AZ	Brask et al. "A Method for Making a Semiconductor Device with a Metal Gate Electrode that is Formed on an Annealed High-K Gate Dielectric Layer", Serial No. Unknown, Filed December 19, 2003					
Examiner			Date Considered				

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Express Mail Label No.: EV 409 362 011 US